Notice of References Cited	Application/Control No. 10/757,788	Applicant(s)/Patent Under Reexamination GOODING ET AL.		
	Examiner Kimberly Thornewell	Art Unit 2128	Page 1 of 1	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,742,181	04-1998	Rush, Kenneth	326/41
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Yu, Shu-Yi. "Fault Tolerance in Adaptive Real-Time Computing Systems." Doctoral Dissertation, Stanford University December 2001.
	V	Babb, Jonathan et al. "Logic Emulation with Virtual Wires." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol. 16 No. 6, June 1997.
	W	Tessier, Russel et al. "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment." MIT Laboratory for Comuter Science 2001.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.